CLAIMS

1. A circuit for providing synchronized transportation of data from a first device having a first clock domain to a second device having a second clock domain, the circuit comprising:

a data register to sample data placed on a data bus by the first device during a first bus clock cycle;

a comparator to compare data on the data bus during a second, consecutive bus clock cycle to the data sampled by the data register;

a multiplexor to output the sampled data to the second device during a third, consecutive bus cycle when the sampled data is equal to the data on the data bus during the second, consecutive bus clock cycle and to output data on the data bus to the second device during the third, consecutive bus clock cycle when the sampled data is not equal to the data on the data bus during the second bus clock cycle.

2. A circuit for providing synchronized transportation of data from a first device having a first clock domain to a second device having a second clock domain, as per claim 1, wherein the first device is an asynchronous peripheral in a computer system and the second device is a bus master.

3. A circuit for providing synchronized transportation of data from a first device having a first clock domain to a second device having a second clock domain, as per claim 1, wherein the first device is maintained in a list indicating that synchronization is needed when data is

transported to the second device and the circuit automatically performs synchronization when the data is transported to the second device.

4. A circuit for providing synchronized transportation of data from a first device having a first clock domain to a second device having a second clock domain, as per claim 1, wherein the first device provides a signal to the circuit to indicate that synchronization is needed when the data is transported to the second device.

5. A circuit for providing synchronized transportation of data from a first device having a first clock domain to a second device having a second clock domain, as per claim 1, wherein the first device provides a signal that indicates a duration of time for transporting data to the second device needs extended.

6. A circuit for providing synchronized transportation of data from a first device having a first clock domain to a second device having a second clock domain, as per claim 1, wherein the first device provides to the circuit a single signal used to both indicate that synchronization is needed and to indicate a duration of time for transporting data to the second device needs extended.

7. A method for providing synchronized transportation of data from a first device having a first clock domain to a second device having a second clock domain, the method comprising:

sampling data placed on a data bus by the first device during a first bus clock cycle;

comparing data on the data bus during a second consecutive bus clock cycle to the sampled data;

for the sampled data equal to the data on the data bus during a second consecutive bus clock cycle, outputting the sampled data to the second device during a third consecutive bus cycle; and

for the sampled data not equal to the data on the data bus during the second consecutive bus clock cycle, outputting data on the data bus during the third consecutive bus clock cycle to the second device.

8. A method for providing synchronized transportation of data from a first device having a first clock domain to a second device having a second clock domain, as per claim 7, wherein the first device is an asynchronous peripheral in a computer system and the second device is a bus master.

9. A method for providing synchronized transportation of data from a first device having a first clock domain to a second device having a second clock domain, as per claim 7, wherein the first device is maintained in a list indicating that synchronization is needed when data is transported to the second device and the circuit automatically performs synchronization when the data is transported to the second device.

10. A method for providing synchronized transportation of data from a first device having a first clock domain to a second device having a second clock domain, as per claim 7, wherein the first device provides a signal to the circuit to indicate that synchronization is needed when the data is transported to the second device.

11. A method for providing synchronized transportation of data from a first device having a first clock domain to a second device having a second clock domain, as per claim 7, wherein the first device provides a signal that indicates a duration of time for transporting data to the second device needs extended.

12. A method for providing synchronized transportation of data from a first device having a first clock domain to a second device having a second clock domain, as per claim 7, wherein the first device provides to the circuit a single signal used to both indicate that synchronization is needed and to indicate a duration of time for transporting data to the second device needs extended.

13. A computer comprising:

an asynchronous peripheral that transmits read data to a bus master by placing the read data on a peripheral bus;

bus interface logic to synchronize the read data, the bus interface logic comprising:

a data register to sample read data on the peripheral bus during a first bus clock cycle;

a comparator to compare read data on the peripheral bus during a second consecutive bus clock cycle to the sampled read data; and

a multiplexor to output the sampled read data during a third consecutive bus cycle when the sampled read data is equal to the read data on the data bus during a second consecutive bus clock cycle and to output read data on the data bus during the third consecutive bus clock cycle when the sampled read data is not equal to the read data on the data bus during a second consecutive bus clock cycle.

14. A computer, as per claim 13, wherein the peripheral is maintained in a list indicating that synchronization is needed for a read access and the bus interface logic automatically performs synchronization when a read access is performed.

15. A computer, as per claim 13, wherein the peripheral provides a signal to the bus logic to indicate that synchronization is needed when a read access is performed.

16. A computer, as per claim 13, wherein the peripheral provides a signal that indicates a duration of time for transporting data to the second device needs extended.

17. A computer, as per claim 13, wherein the peripheral provides to the bus logic a single signal used to both indicate that synchronization is needed and to indicate a duration of time for transporting data to the second device needs extended.